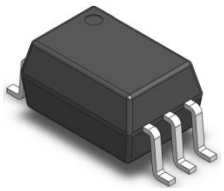
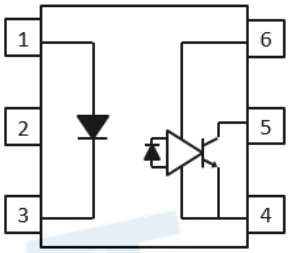
DATASHEET

6 PIN SDIP HIGH SPEED 10MBit/s LOGIC GATE PHOTOCOUPLER
ELS611-G series



Schematic



0.1μF bypass capacitor must be connected between pins 6 and 4 *3

Pin Configuration
1: Anode
2: No Connection
3: Cathode
4: GND
5: V_{out}
6: V_{CC}

Features

- Compliance Halogen Free.
  (Br <900 ppm, Cl <900 ppm, Br+Cl < 1500 ppm).
- Pb free and RoHS compliant
- Compliance with EU REACH.
- High isolation voltage between input and output
  (Viso=5000 Vrms)
- UL and cUL approved (E214129)
- VDE approved (No.254769)
- NEMKO approved
- FIMKO approved
- SEMKO approved
- DEMKO approved
- CQC approved(No.16001145144)

Description

The ELS611-G series devices are consists of an infrared emitting diode optically coupled to a high speed integrated photo detector logic gate with a storable output. The devices in a 6-pin small DIP package.

Applications

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5 volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer peripheral interface

Truth Table (Positive Logic)

Input	Output
H	L
L	H

Absolute Maximum Ratings (Ta=25℃)

Parameter		Symbol	Rating	Unit
Input	Forward current	I_F	20	mA
	Reverse voltage	V_R	5	V
	Power dissipation	P_D	40	mW
Output	Power dissipation	P_C	85	mW
	Output current	I_O	50	mA
	Output voltage	V_O	7.0	V
	Supply voltage	V_{CC}	7.0	V
Output Power Dissipation		P_O	100	mW
Isolation voltage *1		V_{ISO}	5000	V rms
Operating temperature		T_{OPR}	-40 ~ +85	°C
Storage temperature		T_{STG}	-55 ~ +125	°C
Soldering temperature *2		T_{SOL}	260	°C

Notes:
*1 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1, 2, 3are shorted together, and pins 4, 5, 6 are shorted together.

*2 For 10 seconds.

Electrical Characteristics

Input

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward voltage	V_F	-	1.45	1.8	V	I_F = 10mA
Reverse Current	I_R	-	-	10	µA	V_R = 5V
Input capacitance	C_{IN}	-	60	-	pF	V_F=0, f=1MHz

Output

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High Level supply current	I_{CCH}	-	7	13	mA	I_F=0mA, V_{CC}=5.5V
Low Level supply current	I_{CCL}	-	9	15	mA	I_F=10mA, V_{CC}=5.5V

Transfer Characteristics

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High Level Output Current	I_{OH}	-	1	100	uA	V_{CC}=5.5V, V_O=5.5V, I_F=250μA
Low Level Output Current	V_{OL}	-	0.4	0.6	V	V_{CC} = 5.5V, I_F=5mA,I_{OL}=13mA
Input Threshold Current	I_{FT}	-	-	5	mA	V_{CC}= 5.5V, V_O=0.6V, I_{OL}=13mA

Switching Characteristics (V_{CC}=5V, I_F=7.5mA unless specified otherwise)

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Propagation delay time to output High level	T_{PHL}	-	40	100	ns	C_L = 15pF, R_L=350Ω,
Propagation delay time to output Low level	T_{PLH}	-	50	100	ns	C_L = 15pF, R_L=350Ω,
Pulse width distortion	$\|T_{PHL} – T_{PLH}\|$	-	10	50	ns	C_L = 15pF, R_L=350Ω
Output rise time	tr	-	50	-	ns	C_L = 15pF, R_L=350Ω
Output fall time	tf	-	10	-	ns	C_L = 15pF, R_L=350Ω

Switching Characteristics

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Common Mode Transient Immunity at Logic High *4	CM_H	5		-	KV/µS	I_F = 0mA , V_{OH}=2.0V, R_L=350Ω, T_A=25°C V_{CM}=1000Vp-p
Common Mode Transient Immunity at Logic Low *5	CM_L	5	-	-	KV/µS	I_F = 7.5mA , V_{OL}=0.8V, R_L=350Ω, T_A=25°C V_{CM}=1000Vp-p

Typical Electro-Optical Characteristics Curves

Figure 1. Forward Current vs Forward Voltage

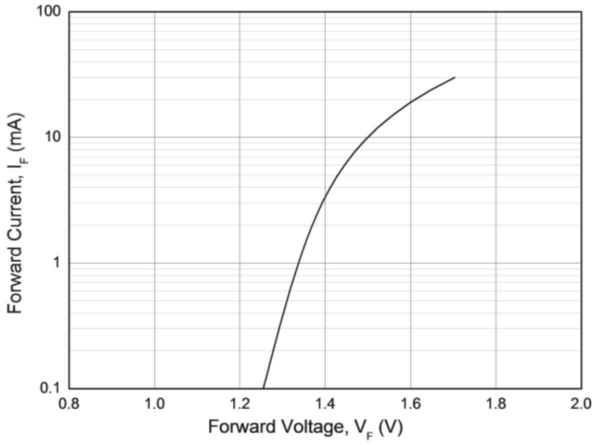


Figure 2. Low Level Output Voltage vs Ambient Temperature

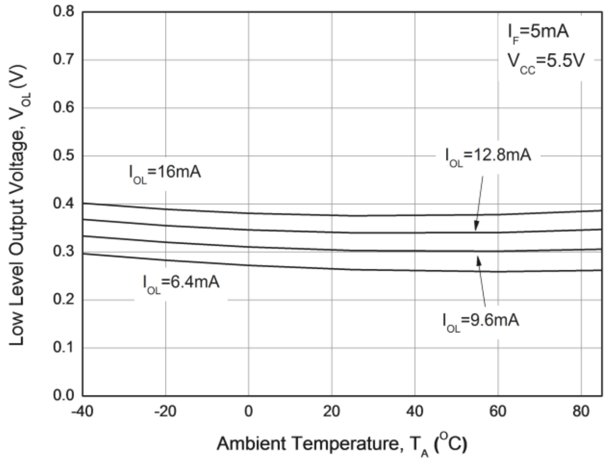


Figure 3. Low Level Output Current vs Ambient Temperature

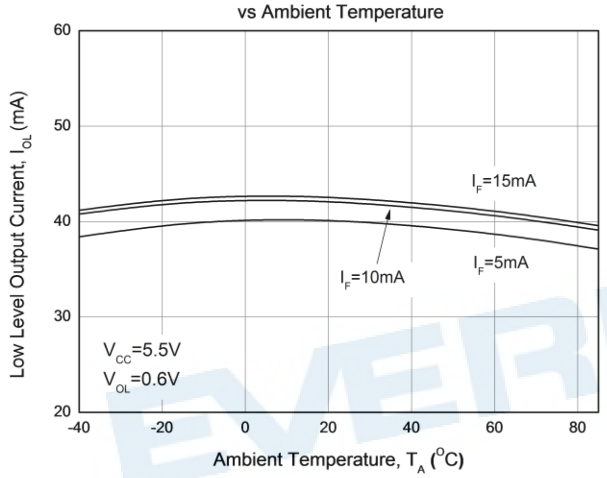


Figure 4. Input Threshold Current vs Ambient Temperature

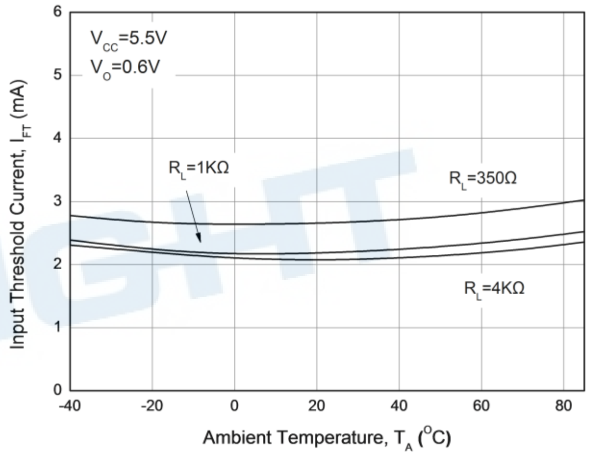


Figure 5. Input Current vs Output Voltage

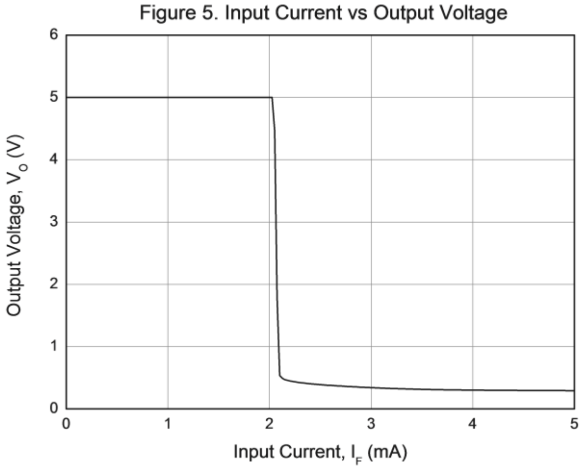


Figure 6. High Level Output Current vs Ambient Temperature

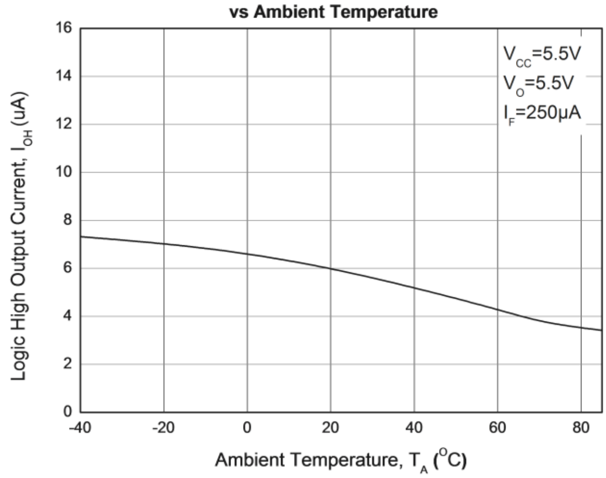


Figure 7. Propagation Delay vs. Forward Current

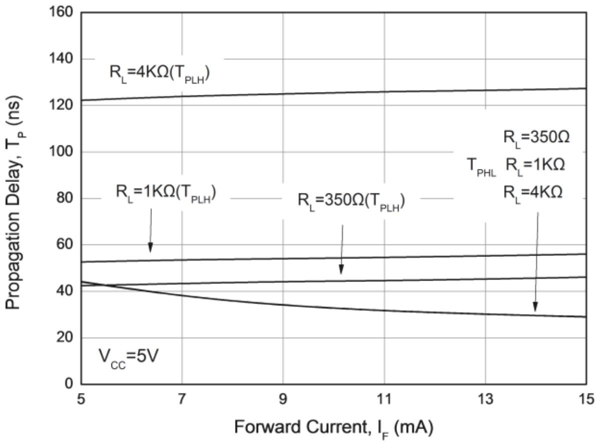


Figure 8. Propagation Delay vs. Temperature

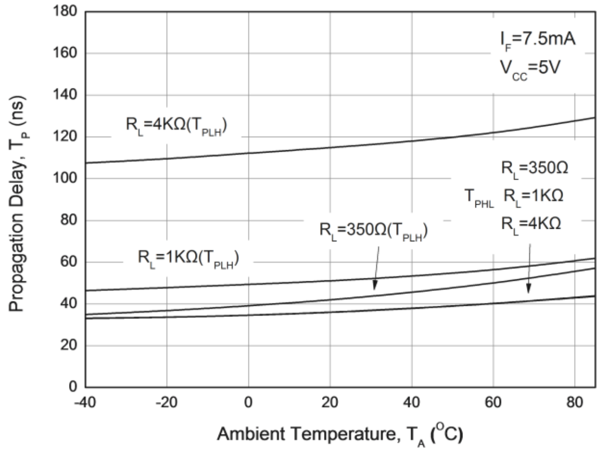


Figure 9. Pulse Width Distortion vs. Temperature

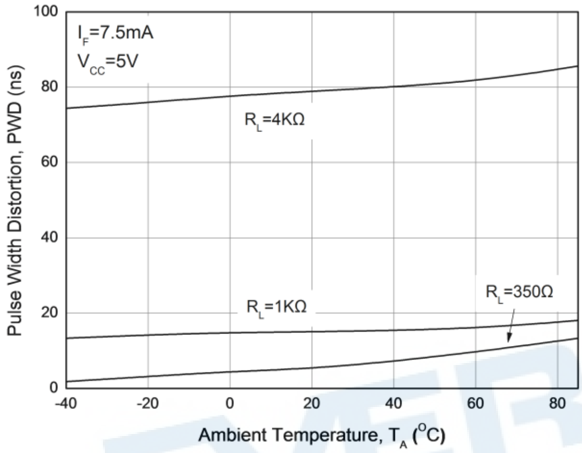


Figure 10. Rise and Fall Time vs. Temperature

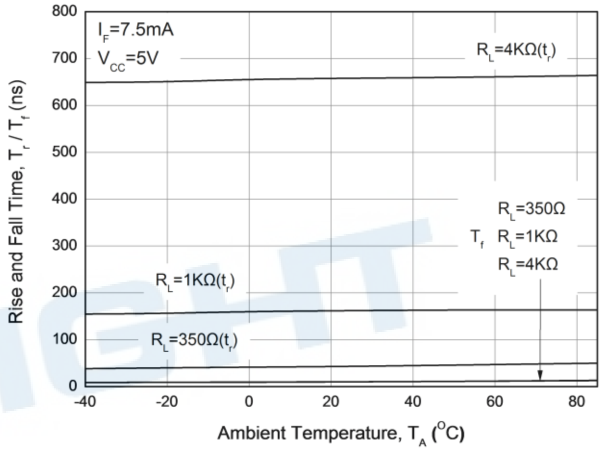


Figure 11. Switching Time Test Circuit & Waveform

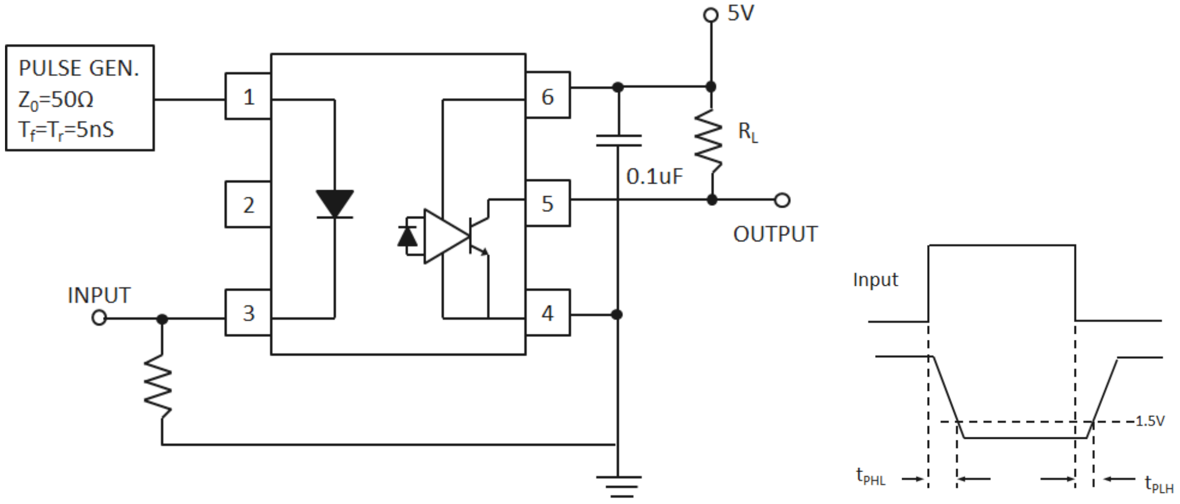
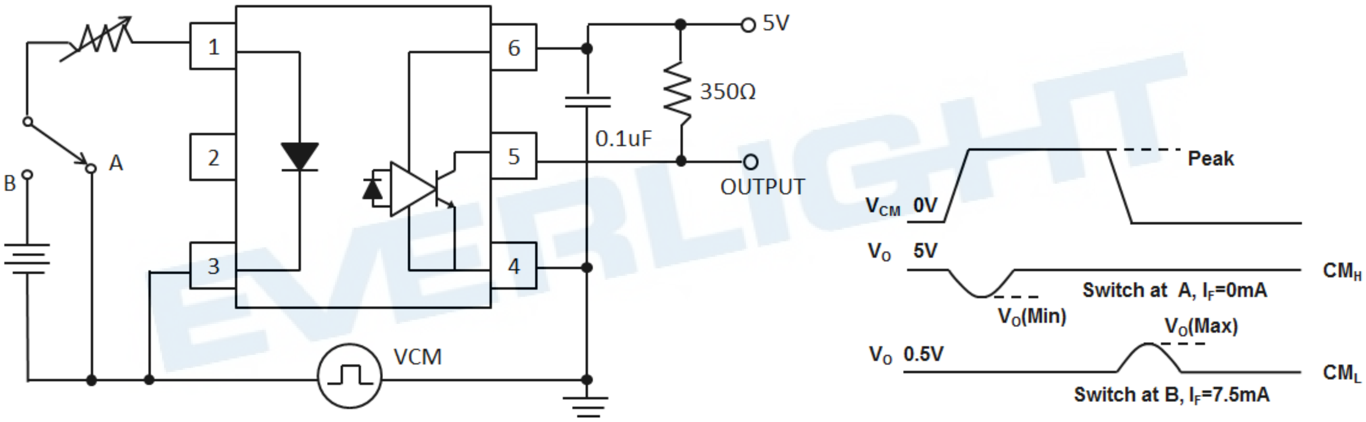


Figure 12. Transient Immunity Test Circuit & Waveform



Note

*3 The V_{CC} supply must be bypassed by a 0.1μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package VCC and GND pins

*4 CM_H– The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., V_{OUT} > 2.0V).

*5 CM_L– The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., V_{OUT} < 0.8V).

Order Information

Part Number

ELS611X(Y)-VG

Note

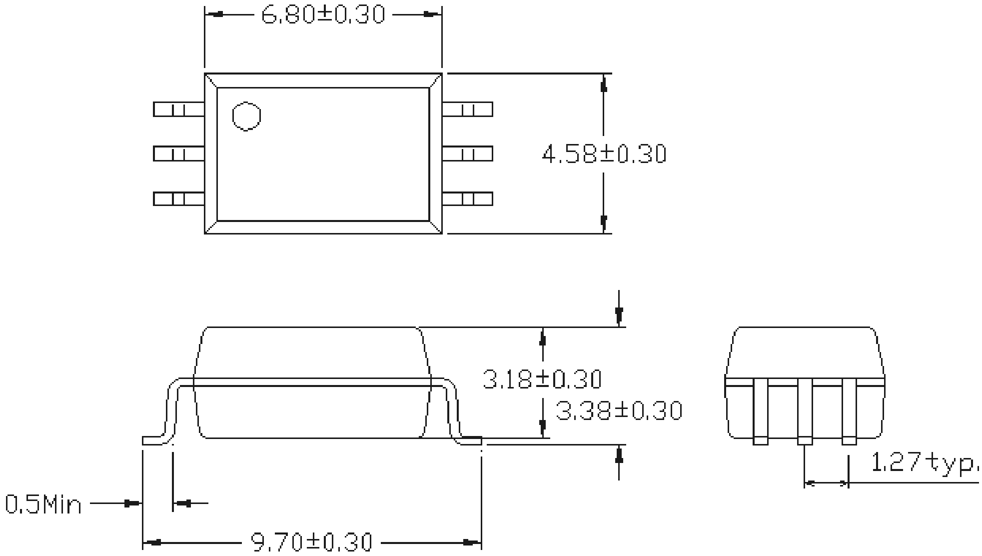
EL = denotes EVERLIGHT
S611 = part no.
X = lead type(P,W)
Y = Tape and reel option (TA, TB)
V = VDE (optional)
G = Halogens free

Option	Description	Packing quantity
P(TA)	Surface mount lead form + TA tape & reel option	1000 units per reel
P(TB)	Surface mount lead form + TB tape & reel option	1000 units per reel
W(TA)	Surface mount lead form + TA tape & reel option	1000 units per reel
W(TB)	Surface mount lead form + TB tape & reel option	1000 units per reel

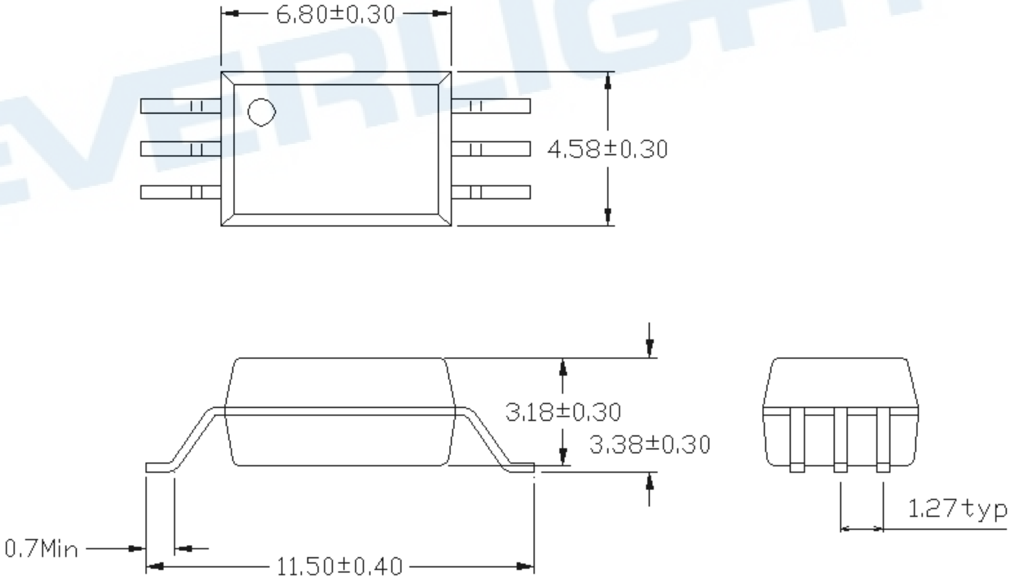
Package Dimension

(Dimensions in mm)

P Type



W Type

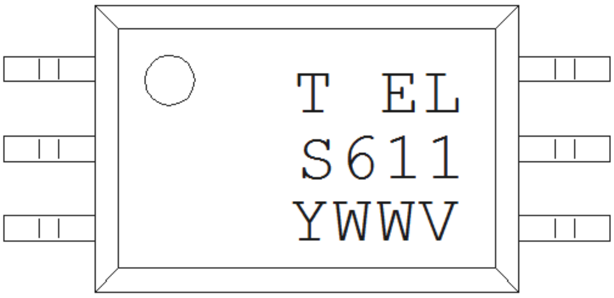


Recommended pad layout for surface mount leadform

For P Type:

For W Type:

Device Marking

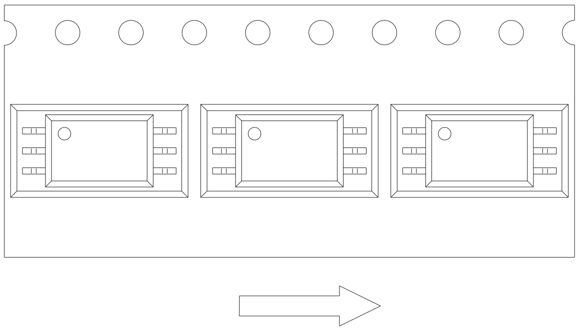


Notes

T	denotes Factory T : made in Taiwan
EL	denotes EVERLIGHT
S611	denotes Device Number
Y	denotes 1 digit Year code
WW	denotes 2 digit Week code
V	denotes VDE (optional)

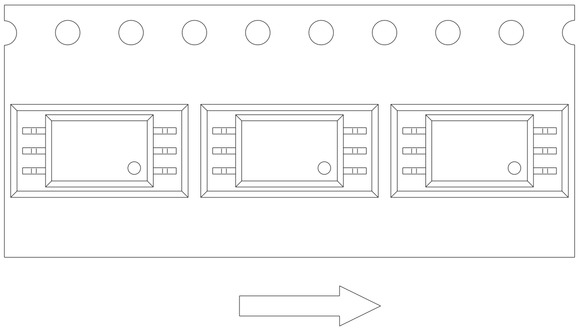
Tape & Reel Packing Specifications

Option TA



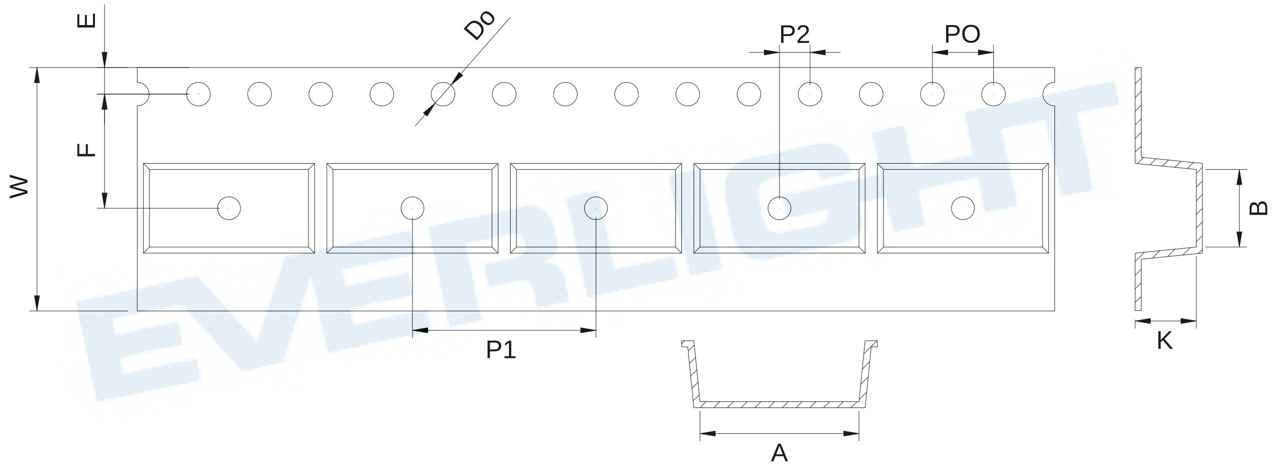
Direction of feed from reel

Option TB



Direction of feed from reel

Tape dimension



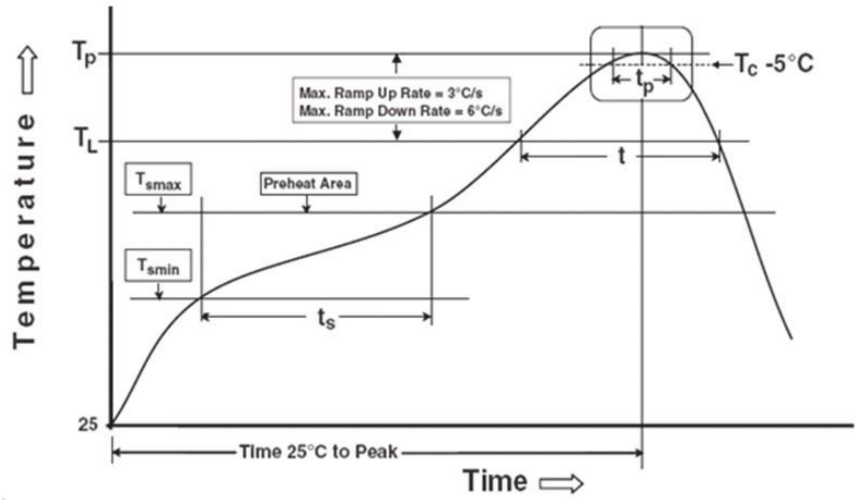
Dimension No.	A	B	Do	E	F	t
Dimension(mm) P	10.4 ± 0.2	4.9 ± 0.2	1.5 ± 0.1	1.75 ± 0.1	7.5 ± 0.1	0.4 ± 0.1
Dimension(mm) W	12.2 ± 0.2	4.9 ± 0.2	1.5 ± 0.1	1.75 ± 0.1	7.5 ± 0.1	0.4 ± 0.1

Dimension No.	PO	P1	P2	W	K
Dimension(mm) P	4.0 ± 0.1	12.0 ± 0.1	2.0 ± 0.1	16.0 ± 0.3	3.7 ± 0.2
Dimension(mm) W	4.0 ± 0.1	16.0 ± 0.1	2.0 ± 0.1	16.0 ± 0.3	3.7 ± 0.2

Precautions for Use

1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile



Note:	Reference: IPC/JEDEC J-STD-020D
Preheat	
Temperature min (T_{smin})	150 °C
Temperature max (T_{smax})	200°C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max
Other	
Liquidus Temperature (T_L)	217 °C
Time above Liquidus Temperature (t_L)	60-100 sec
Peak Temperature (T_P)	260°C
Time within 5 °C of Actual Peak Temperature: T_P - 5°C	30 s
Ramp- Down Rate from Peak Temperature	6°C /second max.
Time 25°C to peak temperature	8 minutes max.
Reflow times	3 times

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