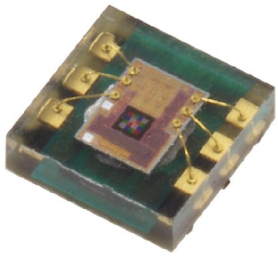
DATASHEET

SMD ▪ I²C Digital RGB Color Sensor
CLS-16D17-34-DF6/TR8



Features

- CMOS technology
- High sensitivity for Red, Green, and Blue light source
- Programmable exposure time
- Convert incident light intensity to digital data
- 16-bit CS ADC resolution
- Automatic light flickering cancellation supporting
- Excellent transmittance of glass package
- Spectral response close to human eye
- Linear CS response for easy design
- Low dark noise
- I²C protocol interface
- Low stop current, 1uA typical
- Operating range 1.7 ~ 3.0V

Description

CLS16D17-34-DF6/TR8 is a digital RGB color sensor that can sense red, green, blue (RGB), and clear light. It can communicate via I²C interface.

Thanks to RGB color sensing, the brightness and color temperature of backlight can be adjusted based on ambient light source that makes the panel look more comfortable for human eyes.

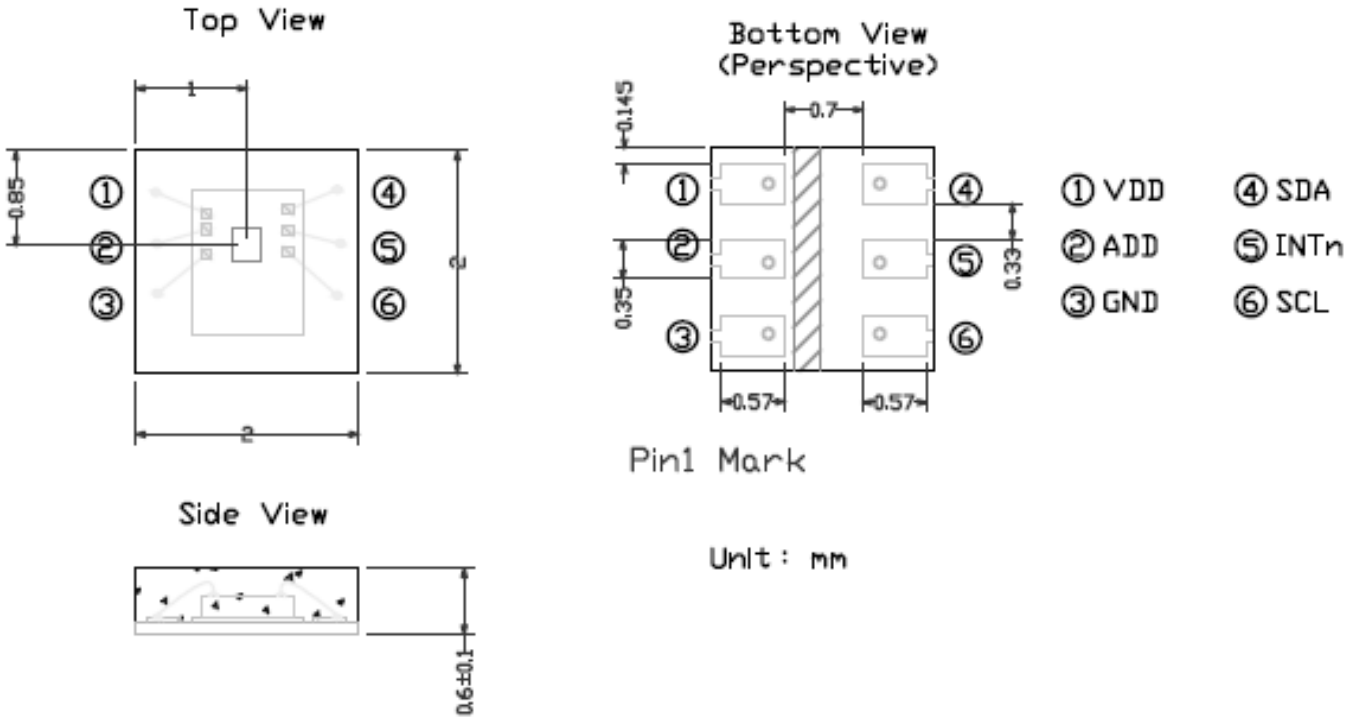
The CS features are ideal for reducing power consumption and adjusting brightness of display equipments like LCD, PDP, LED, virtual keyboard and portable projector, etc.

The operation voltage ranges from 1.7 to 3.0 volt.

Applications

- Digital TV, Tablet PC, Notebook PC
- Navigation systems
- Display-equipped portable devices,etc..

Package Dimensions



Note: Tolerances unless mentioned ±0.1mm. Unit = mm

ADDR	SLAVE ADDRESS
LOW/OPEN	0110_011
HIGH	1001_100

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit.	Remark
VDD	Supply Voltage	0	4.0	V	
Tstg	Storage temperature range	-40	85	°C	
VO	Digital output voltage range	-0.5	4.0	V	
IO	Digital output current	-1	20	mA	
VHBM	ESD tolerance, Human Body Model		2,000	V	

Recommended Operating Condition

Symbol	Parameter	Min	Max	Unit.	Remark
VDD	Supply Voltage	1.7	3.0	V	
TA	Operating temperature	-40	85	°C	
VIL	SCL,SDA input low voltage		600	mV	
VIH	SCL,SDA input low voltage	1.4		V	

Electrical Specifications

Symbol	Parameter	Min	Typ.	Max	Unit.	Remark
V_{DD}	Power Supply	1.7	-	3.0	V	
I_{STOP}	Power Down Current			1	uA	Power Down
I_{DD_CRGB}	Active Current for CRGB	-	400	480	uA	
I_{DD_RGB}	Active Current for RGB	-	320	380	uA	
I_{DD_C}	Active Current for Clear	-	150	180	uA	
F_{OSC}	Internal Oscillator Frequency	-	700	-	kHz	
V_{OL}	INT, SDA output low voltage	0		0.4	V	8mA Sink Current

Optical Characteristics

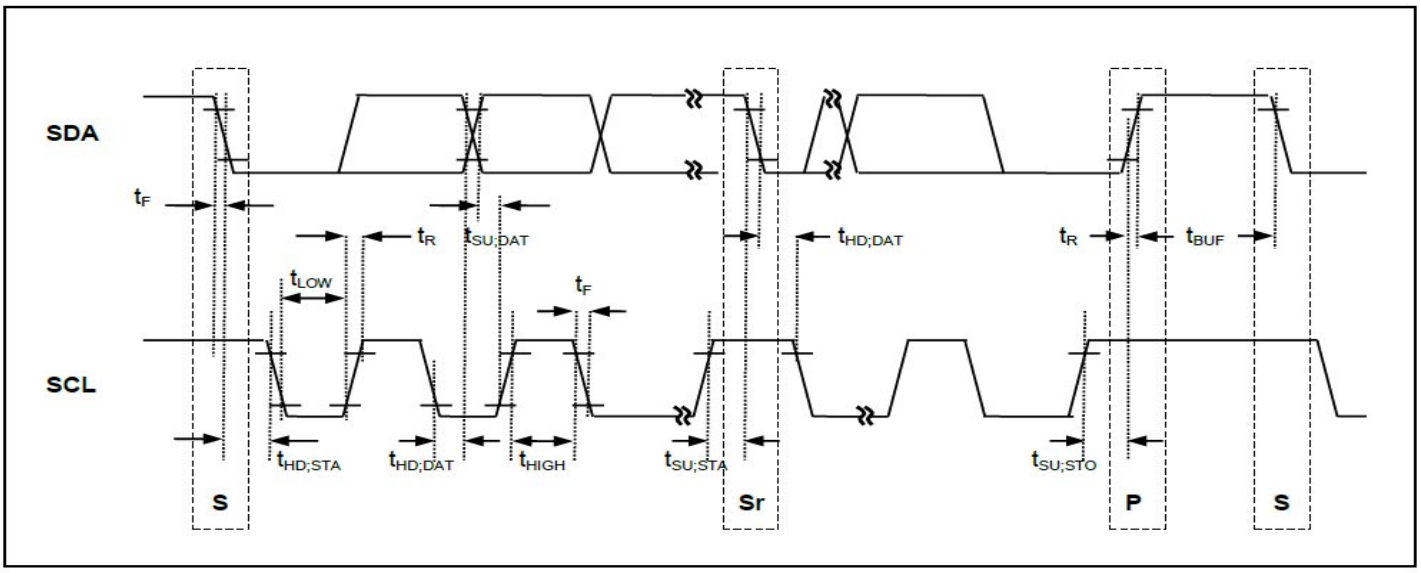
Symbol	Parameter	Min	Typ.	Max	Unit.	Remark
λ_{PC}	Peak Sensitivity wavelength of Clear ADC		615		nm	
λ_{PR}	Peak Sensitivity wavelength of Red ADC		680		nm	
λ_{PG}	Peak Sensitivity wavelength of Green ADC		550		nm	
λ_{PB}	Peak Sensitivity wavelength of Blue ADC		490		nm	
A_C_{000L}	ADC Count Value of Clear channel		0	1	counts	@0lux, white color LED
A_C_{1000L}	ADC Count Value of Red channel	835	806	959	counts	@1000lux, white color LED
A_R_{000L}			0	1	counts	@0lux, white color LED

A_R_{1000L}	ADC Count Value of Green channel	866	967	1108	counts	@1000lux, white color LED
A_G_{000L}			0	1	counts	@0lux, white color LED
A_G_{1000L}	ADC Count Value of Blue channel	531	591	648	counts	@1000lux, white color LED
A_B_{000L}			0	1	counts	@0lux, white color LED
A_B_{1000L}	Full Scale Clear ADC Count	1713	1951	2082	counts	@1000lux, white color LED
DF_{CLEAR}				65535	counts	
DF_{RED}	Full Scale Red ADC Count			65535	counts	
DF_{GREEN}	Full Scale Green ADC Count			65535	counts	
DF_{BLUE}	Full Scale Blue ADC Count			65535	counts	

Parameter	Test Conditions	Red/Clear Channel		Green/Clear Channel		Blue/ Clear Channel	
		Min	Max	Min	Max	Min	Max
Color ADC Count value ratio: Color / Clear	λ_D = 470nm	14%	20%	54%	61%	86%	92%
	λ_D = 525nm	16%	19%	75%	79%	56%	62%
	λ_D = 624nm	100%	109%	30%	32%	9%	10%

I²C Characteristics

Parameter	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time after (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	-	us
LOW period of the SCL clock	t_{LOW}	1.3	-	us
HIGH period of the SCL clock	t_{HIGH}	0.6	-	us
Setup time for a repeated START condition	$t_{SU;STA}$	0.6	-	us
Data hold time	$t_{HD;DAT}$	0	0.9	us
Data setup time	$t_{SU;DAT}$	100	-	ns
Clock/data fall time	t_F	0	300	ns
Clock/data rise time	t_R	0	300	ns
Setup time for STOP condition	$t_{SU;STO}$	0.6	-	us
Bus free time between a STOP and START condtion	t_{BUF}	1.3	-	us



Definition of timing for fast mode devices on the I2C bus

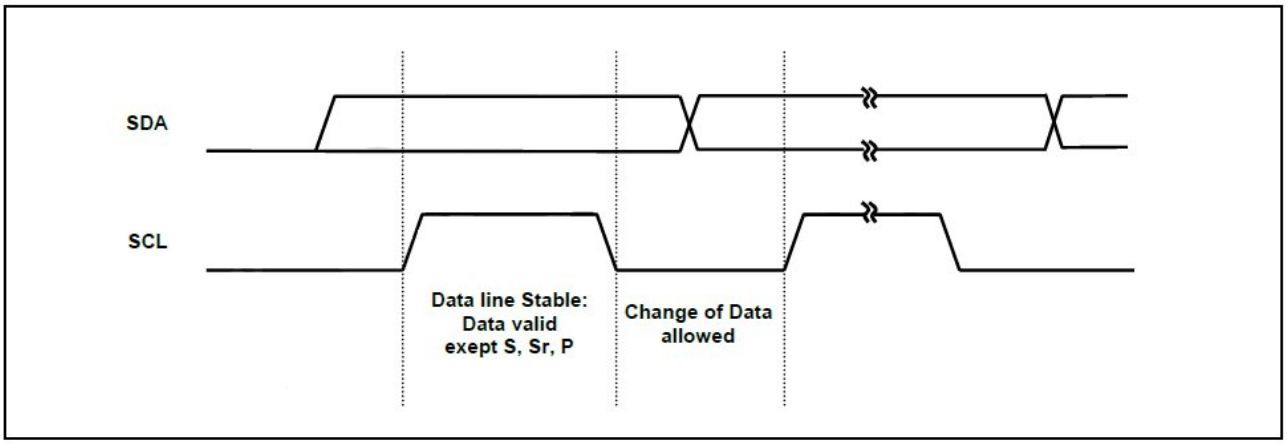
I²C Operation Overview

The I²C is one of industrial standard serial communication protocols, and which uses 2 bus lines Serial Data Line (SDA) and Serial Clock Line (SCL) to exchange data. Because both SDA and SCL lines are open-drain output, each line needs pull-up resistor. The features are as shown below.

- Compatible with I²C interface
- Up to 400kHz data transfer speed
- Support two 7-bit slave address
- Slave operation only

I²C Bit Transfer

The data on the SDA line must be stable during HIGH period of the clock, SCL. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. The exceptions are START(S), repeated START(Sr) and STOP(P) condition where data line changes when clock line is high.



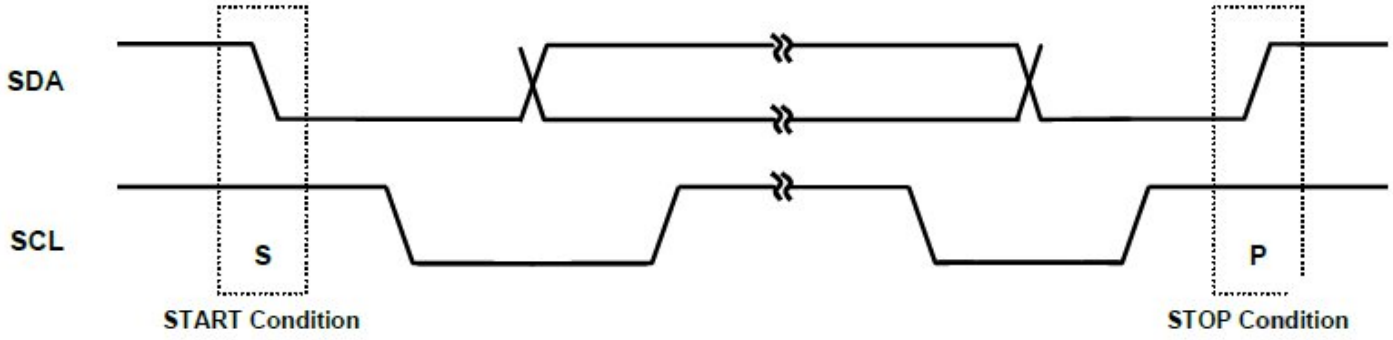
Bit Transfer on the I²C-Bus

Start / Repeated Start / Stop

One master can issue a START (S) condition to notice other devices connected to the SCL, SDA lines that it will use the bus. A STOP (P) condition is generated by the master to release the bus lines so that other devices can use it.

- A high to low transition on the SDA line while SCL is high defines a START (S) condition.
- A low to high transition on the SDA line while SCL is high defines a STOP (P) condition.

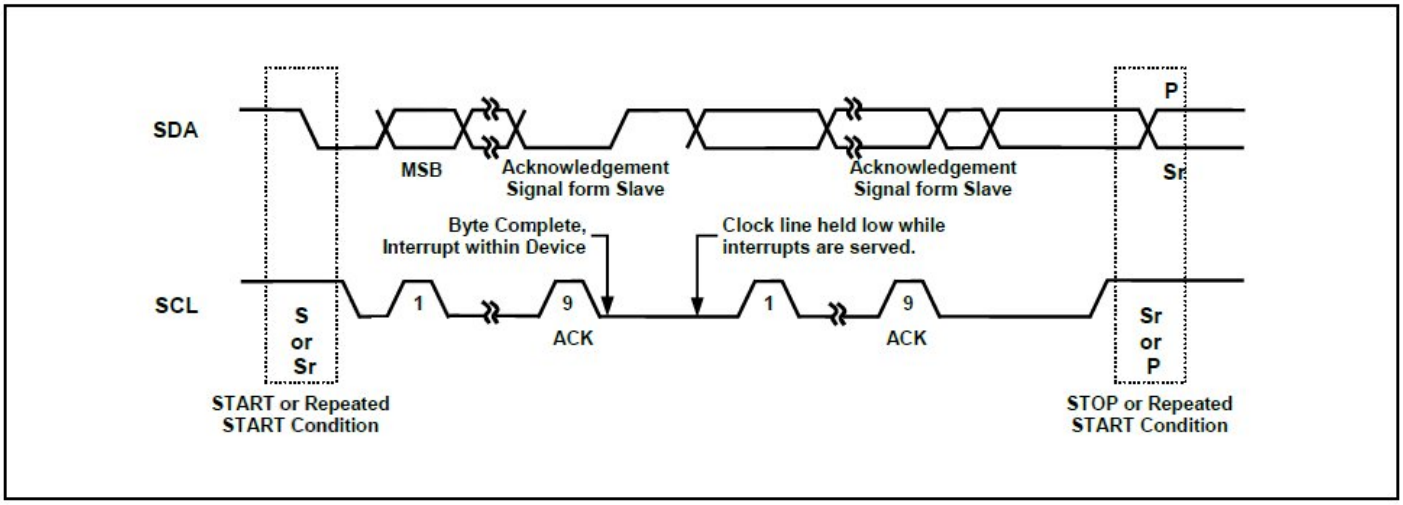
START and STOP conditions are always generated by a master. The bus is considered to be busy after START condition. The bus is considered to be free again after STOP condition, ie, the bus is busy between START and STOP condition. If a repeated START condition (Sr) is generated instead of STOP condition, the bus stays busy. So, the START and repeated START conditions are functionally identical.



START and STOP Condition

Data Transfer

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unlimited. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave can't receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

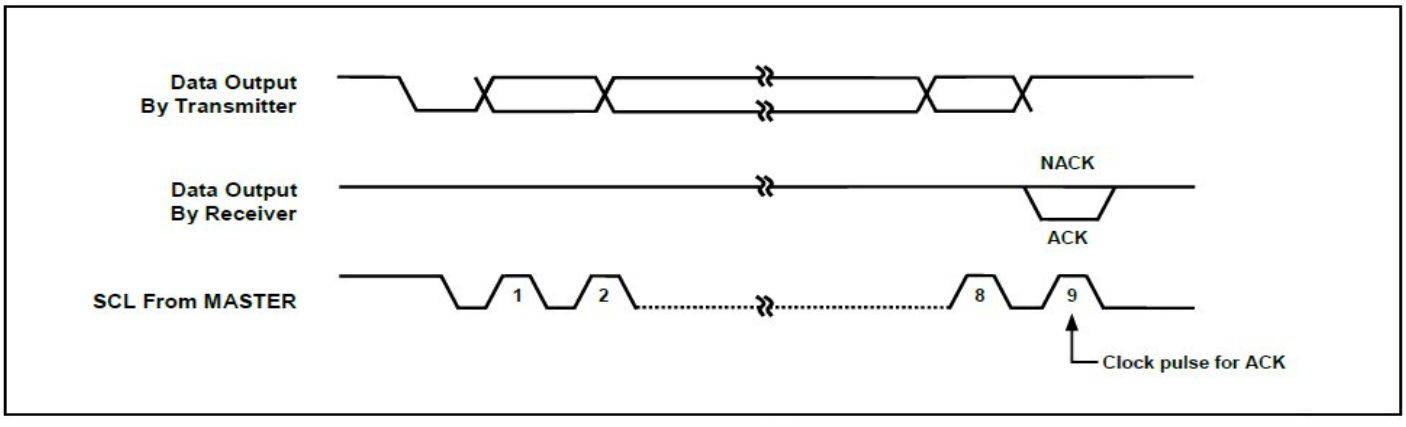


STOP or Repeated START Condition

Acknowledge

The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. When a slave is addressed by a master (Address Packet), and if it is unable to receive or transmit because it's performing some real time function, the data line must be left HIGH by the slave. And also, when a slave addressed by a master is unable to receive more data bits, the slave receiver must release the SDA line (Data Packet). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate a STOP or repeated START condition.



Acknowledge on the I²C-Bus

Operation

The I²C is byte-oriented serial protocol and data transfer between master and this slave device is initiated by a start condition(S) from master. After start condition, the master sends 7-bit slave address and 1-bit read-write control bit. We call these 8-bit data address packet. The next bytes followed by address packet are all data packet unless another start condition is detected before a stop condition.

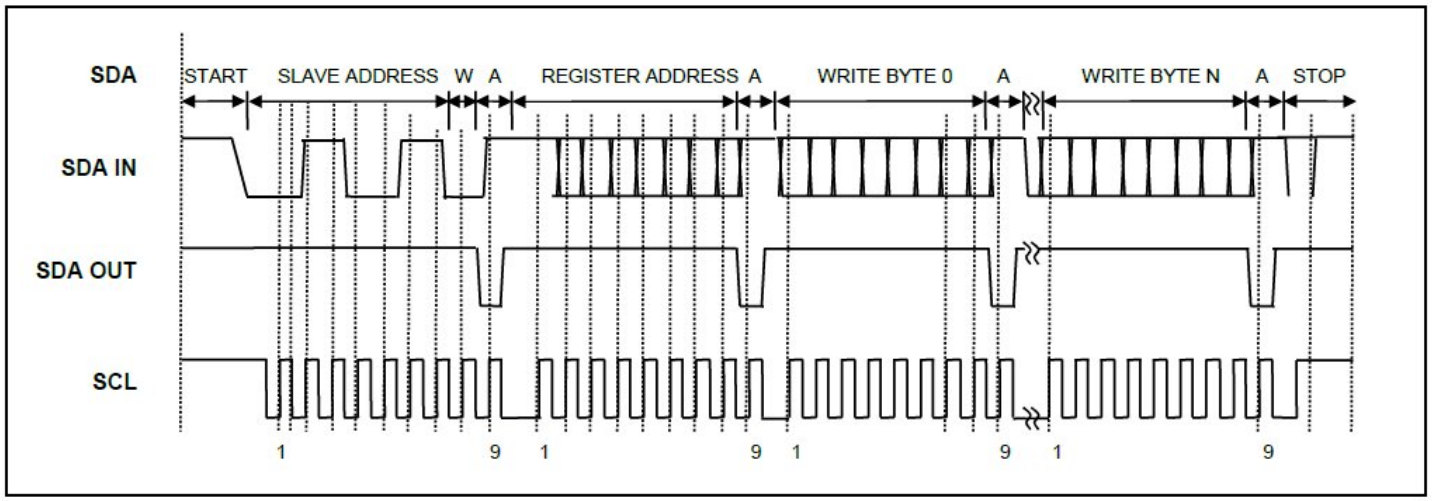
The 2nd byte sent from master after address packet with write direction is interpreted as base register or memory address byte. And this base address is incremented only when master transmits more than 2 bytes after start condition because the 2nd byte is register address field.

The color sensor's I²C slave address is configured as "0110011B" or "1001100B" according to the input condition of ADDR pin.

Write Protocol (Master Transmitter)

The master transmits a start condition(S), slave address and Write bit. If the high 7-bits of address packet equal to the device's slave address, the color sensor acknowledges by pulling down the SDA line at the 9th SCL clock period. After address packet and acknowledge bit, the master transmits a data which is used for base address accessing internal memory or register of the device. The master transmits a number of data to be written and the slave always acknowledges for every data received. To finish transfer the master sends a stop condition regardless of the acknowledgement.

The destination address for incoming data byte increments automatically by one data packet. For example, if master transmits 5 data bytes including a base address(=register address in the following figure) byte and the base address is configured as 00H, the internal address is defined as 00H for 1st data byte, 01H for 2nd data byte, 02H for 3rd data byte and 03H for 4th data byte. This applies to Read Protocol also.



I2C Write Protocol

Registers

The Color Sensor is controlled and monitored by 19 registers. These registers provide a variety of control functions and can be read to determine results of the ADC conversions.

Name	Address	Dir	Default	Description
ADDRSET	-	W		Address Set Register
CONTROL	00_H	R/W	00_H	Control Register
INTR	01_H	R/W	00_H	Interrupt Control Register
RGBCON	02_H	R/W	01_H	RGB mode control Register
WTIME	05_H	R/W	01_H	Wait Time Register
CILTL	06_H	R/W	00_H	CS Interrupt Low Threshold Low Register
CILTH	07_H	R/W	00_H	CS Interrupt Low Threshold High Register
CIHTL	08_H	R/W	FF_H	CS Interrupt High Threshold Low Register
CIHTH	09_H	R/W	FF_H	CS Interrupt High Threshold High Register
PERSIST	$0E_H$	R/W	11_H	Interrupt Persistence Register
ID	11_H	R	$E0_H$	Revision Number read Register
CDATAL	12_H	R	00_H	Clear ADC Data Low Register
CDATAH	13_H	R	00_H	Clear ADC Data High Register
RDATAL	14_H	R	00_H	Red ADC Data Low Register
RDATAH	15_H	R	00_H	Red ADC Data High Register
GDATAL	16_H	R	00_H	Green ADC Data Low Register
GDATAH	17_H	R	00_H	Green ADC Data High Register
BDATAL	18_H	R	00_H	Blue ADC Data Low Register
BDATAH	19_H	R	00_H	Blue ADC Data High Register
AGC	$1E_H$	R/W	01_H	ADC Gain control Register

Registers Descripion

ADDRSET (Address Set Register) --H

7	6	5	4	3	2	1	0
-	-	-	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
-	-	-	R/W	R/W	R/W	R/W	R/W

Initial value : 00_H

ADDR[4:0] Base address for subsequent register access. When the I2C master initiates a write protocol with start bit and slave address transfer, the second byte is used to configure register address.

CONTROL (Control Register) 00_H

7	6	5	4	3	2	1	0
SOFTRST	CTCON1	CTCON0	- NOTE1	MODE2	MODE1	MODE0	POWER
R/W	R/W	R/W	-	R/W	R/W	R/W	R/W

Initial value : 00_H

SOFTRST Soft reset. This bit is auto-cleared.

0 No operation

1 Reset internal registers

ATCON[1:0] CS Integration time(CTIME) select. This bit field is used with IT_CON in RGBCON register.

CTCON[1:0]	IT_ CON=0	IT_CON=1
00	12.5ms	800ms
01	25ms	400ms
10	50ms	200m
11	100ms	100ms

MODE[2:0] Control CS Operating Mode. *note2*

000	No operation
100	Clear
101	Clear + R
001	Red
101	Green
011	Blue
110	R/G/B
111	Clear + R/G/B

POWER Power On Enables internal RC oscillator(Typically 700kHz)

0 Turns off the color sensor

1 Turns on the color sensor

NOTE1 Do not write '1' to this bit filed for proper operation.

NOTE2 The real MODE[2:0] bits are updated after internal oscillator is enabled. So reading CONTROL register will return "---- 0000B" when writing '1' to these bits while POWER bit is disabled or enabling MODE[2:0] and POWER bits simultaneously.

By controlling MODE[2:0] bits individually, color sensor can operate as a single channel or multi channel CS.

INTR (Interrupt Control Register) 01_H

7	6	5	4	3	2	1	0
-	-	CINTF	INTEDGE	- NOTE	CINTEN	RGBSEL1	RGBSEL0
-	-	R	RW	-	RW	RW	RW

Initial value : 00_H

CINTF CS Interrupt Flag. Indicates that the device is asserting an interrupt.
This bit is read-only, but writing 0 to this bit clears CINTF flag.
0 No Interrupt or interrupt cleared.
1 ALS interrupt requested.

INTEDGE Interrupt signal is triggered as pulse type at rising edge of internal clock,typically 1.4us period. The host needs not to clear interrupt.
0 Level interrupt
1 Edge interrupt

CINTEN Enablees CS Interrupt generation
0 CS interrupt output is disabled.
1 CS interrupt occurs on/INT pin.

RGBSEL[1:0] CS Interrupt Source Select.
RGBSEL[1:0]
00 Clear channel
01 Red channel
10 Green channel
11 IR channel

NOTE Do not write '1' to this bit filed for proper operation.

RGBCON (RGB mode control Register) 02_H

7	6	5	4	3	2	1	0
CGAIN1	CGAIN0	IT_CON	-	-	-	- NOTE	- NOTE
RW	RW	RW	-	-	-	-	-

Initial value : 01_H

CGAIN[1:0] CS ADC Gain Select. The gain is common for all C/R/G/B ADC channels.
CGAIN[1:0]
00 16x
01 1x
10 4x
11 64x

IT_CON Specifies the CS integration time range.

0 CS integration time ranges from 12.5ms to 100ms.
1 CS integration time ranges from 100ms to 800ms.

NOTE Do not write '1' to this bit filed for proper operation.

WTIME (Wait Time Register) 05_H

7	6	5	4	3	2	1	0
ONESHOT	WTIME6	WTIME5	WTIME4	WTIME3	WTIME2	WTIME2	WTIME1
RW	RW	RW	RW	RW	RW	RW	RW

Initial value : 01_H

ONESHOT Stops ADC integration on completion of one integration cycle.

0 Continuous operation.

1 Once an integration cycle is over, all CS ADC channels will automatically stop and also the MODE[2:0] bits in CONTROL register is to be cleared. To resume operation, re-assert one of MODE[2:0] bits.

MTIME[6:0] Wait Time. Specifies the wait time between continuous CS operations in 5ms interval.

Wait time = 5ms x WTIME[6:0]

The maximum wait time is about 635ms (1111111B).

0000000	No wail
0000001	5ms
0000010	10ms
0001010	50ms
0010100	100ms
0101000	200ms
1010000	400ms
1111111	635ms

The WTIME is used to reduce average power consumption, because the CS ADC stop integrating during wait time period.

When MODE[2:0]!=000B, the internal operating state machine repeats CS and WAIT state continuously. The internal operating mode is as follows : CS—WAIT—CS—WAIT—CS—WAIT…

CAUTION Although setting a larger wait time contributes to reduce average consumption current, it makes update period and response time longer.

CILTL (CS Interrupt Low Threshold Low Register) 06_H

7	6	5	4	3	2	1	0
CILTL7	CILTL6	CILTL5	CILTL4	CILTL3	CILTL2	CILTL1	CILTL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00_H

CILTL[7:0] CS ADC channel interrupt low threshold low register.

CILTH (CS Interrupt Low Threshold High Register) 07_H

7	6	5	4	3	2	1	0
CILTH7	CILTH6	CILTH5	CILTH4	CILTH3	CILTH2	CILTH1	CILTH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00_H

CILTH[7:0] CS ADC channel interrupt low threshold high register.

CIHTL (CS Interrupt High Threshold Low Register) 08_H

7	6	5	4	3	2	1	0
CIHTL7	CIHTL6	CIHTL5	CIHTL4	CIHTL3	CIHTL2	CIHTL1	CIHTL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FF_H

CIHTL[7:0] CS ADC channel interrupt high threshold low register.

CIHTH (CS Interrupt High Threshold High Register) 09_H

7	6	5	4	3	2	1	0
CIHTH7	CIHTH6	CIHTH5	CIHTH4	CIHTH3	CIHTH2	CIHTH1	CIHTH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FF_H

The interrupt threshold registers store the values to be used as the high and low trigger points for the adc data registers. If the value of adc data register crosses below or equal to the low threshold specified, an interrupt can be asserted on the interrupt pin. Likewise, if the result from ADC conversion crosses above the high threshold specified, an interrupt can be asserted on the interrupt pin.

These high and low threshold registers are all 16-bit wide and the concatenated CILTH and CILTL is used as interrupt low threshold(=CILT) and the concatenated CIHTH and CIHTL is used as interrupt high threshold(=CIHT).

PERSIST (Interrupt Persistence Register) 0E$_H$

7	6	5	4	3	2	1	0
-	-	-	-	CPER3	CPER2	CPER1	CPER0
-	-	-	-	R/W	R/W	R/W	R/W

Initial value : 11$_H$

CPER[3:0] CS Interrupt persistence. These bit field control the rate of CS interrupt request to host chip.

CPER[3:0]

0000	Every ALS cycle generates an interrupt.
0001	1 consecutive ALS ADC value out of range.
0010	2 consecutive ALS ADC value out of range.
...	...
1111	15 consecutive ALS ADC value out of range.

NOTE Do not write '1' to this bit filed for proper operation.

ID (Revision ID read Register) 11$_H$

7	6	5	4	3	2	1	0
-	-	-	-	-	-	REVNO1	REVNO0
-	-	-	-	-	-	R	R

Initial value : E0$_H$

REVNO[1:0] Revision ID read

CDATAL (ALS Clear CH ADC Data Low Register) 12$_H$

7	6	5	4	3	2	1	0
CDATAL7	CDATAL6	CDATAL5	CDATAL4	CDATAL3	CDATAL2	CDATAL1	CDATAL0
R	R	R	R	R	R	R	R

Initial value : 00$_H$

CDATAL[7:0] CS Clear CH ADC channel data low register.

The ALS ADC is of 16-bit resolution, and the integrated values appear on four registers C/R/G/B/IR respectively. All ALS ADC data registers are read-only.

CDATAH (ALS Clear CH ADC Data High Register) 13$_H$

7	6	5	4	3	2	1	0
CDATAH7	CDATAH6	CDATAH5	CDATAH4	CDATAH3	CDATAH2	CDATAH1	CDATAH0
R	R	R	R	R	R	R	R

Initial value : 00$_H$

CDATAH[7:0] CS Clear CH ADC channel data high register.

RDATAL (ALS Red CH ADC Data Low Register) 14_H

7	6	5	4	3	2	1	0
RDATAL7	RDATAL6	RDATAL5	RDATAL4	RDATAL3	RDATAL2	RDATAL1	RDATAL0
R	R	R	R	R	R	R	R

Initial value : 00_H

RDATAL[7:0] CS Red CH ADC channel data low register.

RDATAH (ALS Red CH ADC Data High Register) 15_H

7	6	5	4	3	2	1	0
RDATAH7	RDATAH6	RDATAH5	RDATAH4	RDATAH3	RDATAH2	RDATAH1	RDATAH0
R	R	R	R	R	R	R	R

Initial value : 00_H

RDATAH[7:0] CS Red CH ADC channel data high register.

GDATAL (ALS Green CH ADC Data Low Register) 16_H

7	6	5	4	3	2	1	0
GDATAL7	GDATAL6	GDATAL5	GDATAL4	GDATAL3	GDATAL2	GDATAL1	GDATAL0
R	R	R	R	R	R	R	R

Initial value : 00_H

GDATAL[7:0] CS Green CH ADC channel data low register.

GDATAH (ALS Green CH ADC Data High Register) 17_H

7	6	5	4	3	2	1	0
GDATAH7	GDATAH6	GDATAH5	GDATAH4	GDATAH3	GDATAH2	GDATAH1	GDATAH0
R	R	R	R	R	R	R	R

Initial value : 00_H

GDATAH[7:0] CS Green CH ADC channel data high register.

BDATAL (ALS Blue CH ADC Data Low Register) 18_H

7	6	5	4	3	2	1	0
BDATAL7	BDATAL6	BDATAL5	BDATAL4	BDATAL3	BDATAL2	BDATAL1	BDATAL0
R	R	R	R	R	R	R	R

Initial value : 00_H

BDATAL[7:0] CS Blue CH ADC channel data low register.

BDATAH (ALS Blue CH ADC Data High Register) 19_H

7	6	5	4	3	2	1	0
BDATAH7	BDATAH6	BDATAH5	BDATAH4	BDATAH3	BDATAH2	BDATAH1	BDATAH0
R	R	R	R	R	R	R	R

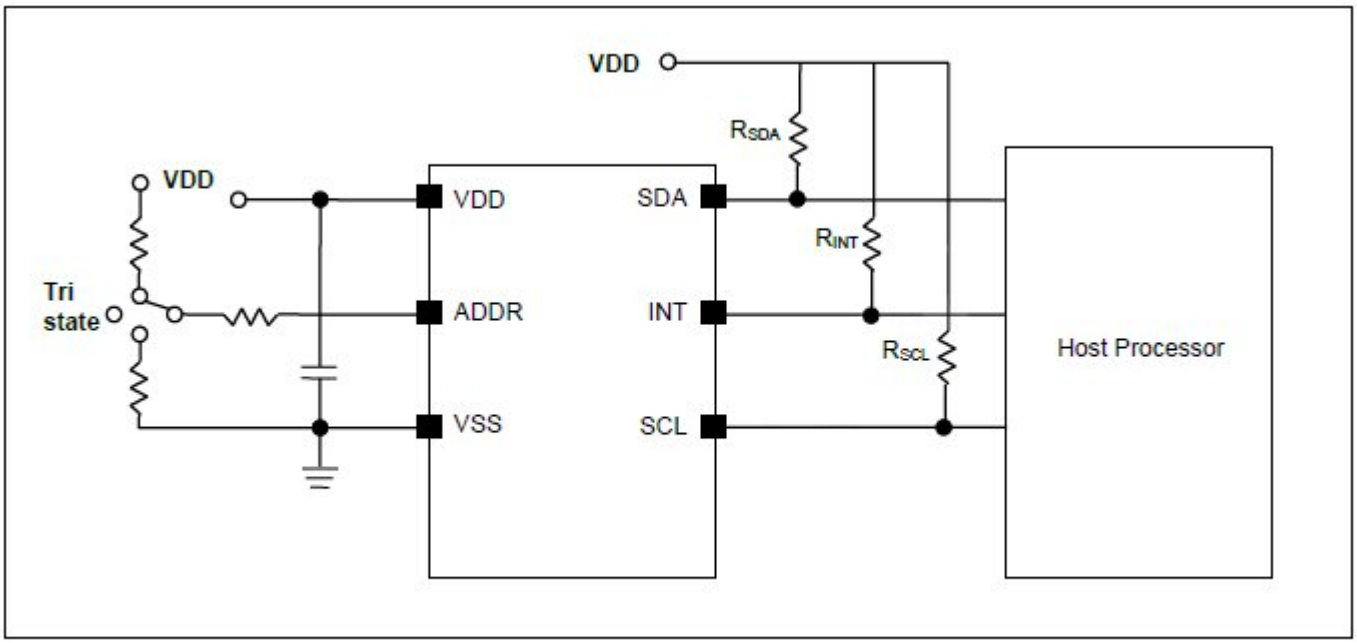
Initial value : 00_H

BDATAH[7:0] CS Blue CH ADC channel data high register.

Appendix

Brief Application Note

A capacitor should be located close to VDD pin of color sensor to reduce power noise. The pull up resistors of two line serial bus are recommended to be around 10kΩ, especially a pull up registor for INT connected to host controller must be 100kΩ.



Hardware pin connection diagram

Notice

1) Operation voltage 1.7 to 3.0V

2) Set SLAVE address (Determined by ADDR pin condition during power-up)

Input Low : 0x33(0110011) => In Master IIC situation when writing and its value is 0x66 and when reading , its value is 0x67

Input High : 0x4C(1001100) => In Master IIC situation when writing, value is 0x98 and when reading, value is 0x99

Floating : 0x33(0110011) => In Master IIC situation when writing, value is 0x66 and when reaing, value is 0x67

3) IIC speed is the standard, about 100kHz.

When writing IIC Multi bytes (Single byte read and write rarely is used)

- Multi bytes Writing :

START(M)+SlaveAddress_W(0x66,M)+ACK(S)+REG_ADDR(0xxx,M)+ACK(S)+WRITE_BYTE0+ACK(S)…+STOP(M)